ABSTRACT

An in-order issue in-order completion micro-controller comprises a pipeline core comprising in succession a fetch address stage, a program access stage, a decode stage, a first execution stage, a second execution stage, a memory access stage, and a write back stage. The various stages are provided a thread ID such that alternating stages use a first thread ID, and the other stages use a second thread ID. Each stage which requires access to thread ID specific context information uses the thread ID to specify this context information.